

<b>Notice of References Cited</b>	Application/Control No. 10/721,260	Applicant(s)/Patent Under Reexamination SAKATA, TOYOKAZU	
	Examiner Patricia A. George	Art Unit 1765	Page 1 of 1

**U.S. PATENT DOCUMENTS**

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-2003/0181034	09-2003	Jiang et al.	438/638
*	B	US-4,931,144	06-1990	Brighton, Jeffrey E.	174/262
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

**FOREIGN PATENT DOCUMENTS**

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

**NON-PATENT DOCUMENTS**

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Lin et al.; An Optimized Integration Scheme for 0.13 um Technology Node Dual-Damascene Cu Interconnect; 0-7803-6327—2/00 © 2000 IEEE
	V	
	W	
	X	

\*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)  
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